Coherent Logix™
Enabling Low Power Software Defined Systems™

Portland, OR

San Jose, CA

Austin, TX

Coherent Logix, Incorporated

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Building 3, Suite 310

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Maker of ultra low-power, extremely-high performance, C-programmable processors (HyperX™) and RF chipsets (*rf*X™) for the embedded systems market – enabling low-power, real-time software defined systems.

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Chief Technology Officer

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Wireless
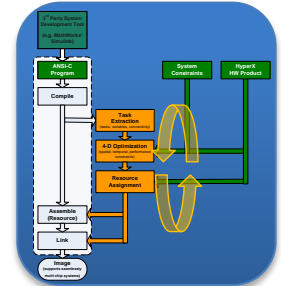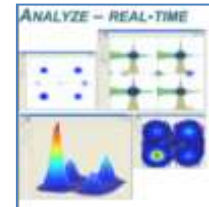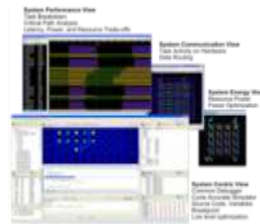
Image / Video

Mil / Aero

High-Rel / Rad-Tol

Research Areas:
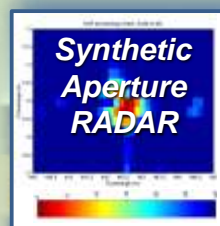## *Market Application requirements driving programmable development solutions to product*

software development tool solutions

system development to hardware product solutions

Enabling Systems for the Warfighter
Low Power • High Performance • Portable • Battery Operated

Synthetic Aperture RADAR

MUOS

NASA

DARPA

LINK-16

JAN-TE
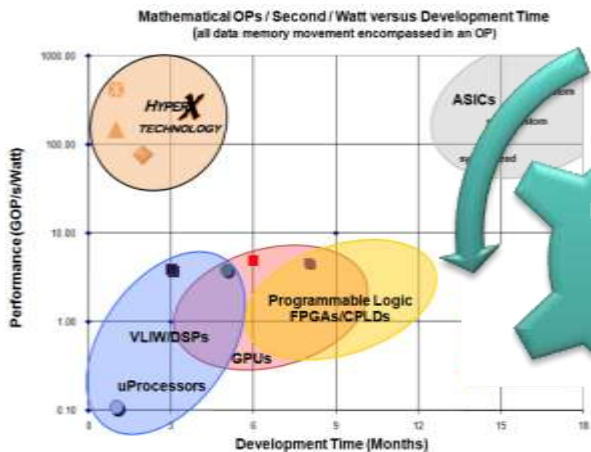
WNW

SRW

Hyperspectral Multispectral Fusion

- ❑ *Software Defined Radio*
- ❑ *Software Defined GPS*
- ❑ *Anti-jam GPS*
- ❑ *Surveillance Receiver*
- ❑ *Hyperspectral Imaging*
- ❑ *Multi-spectral Data Fusion*
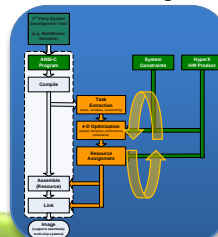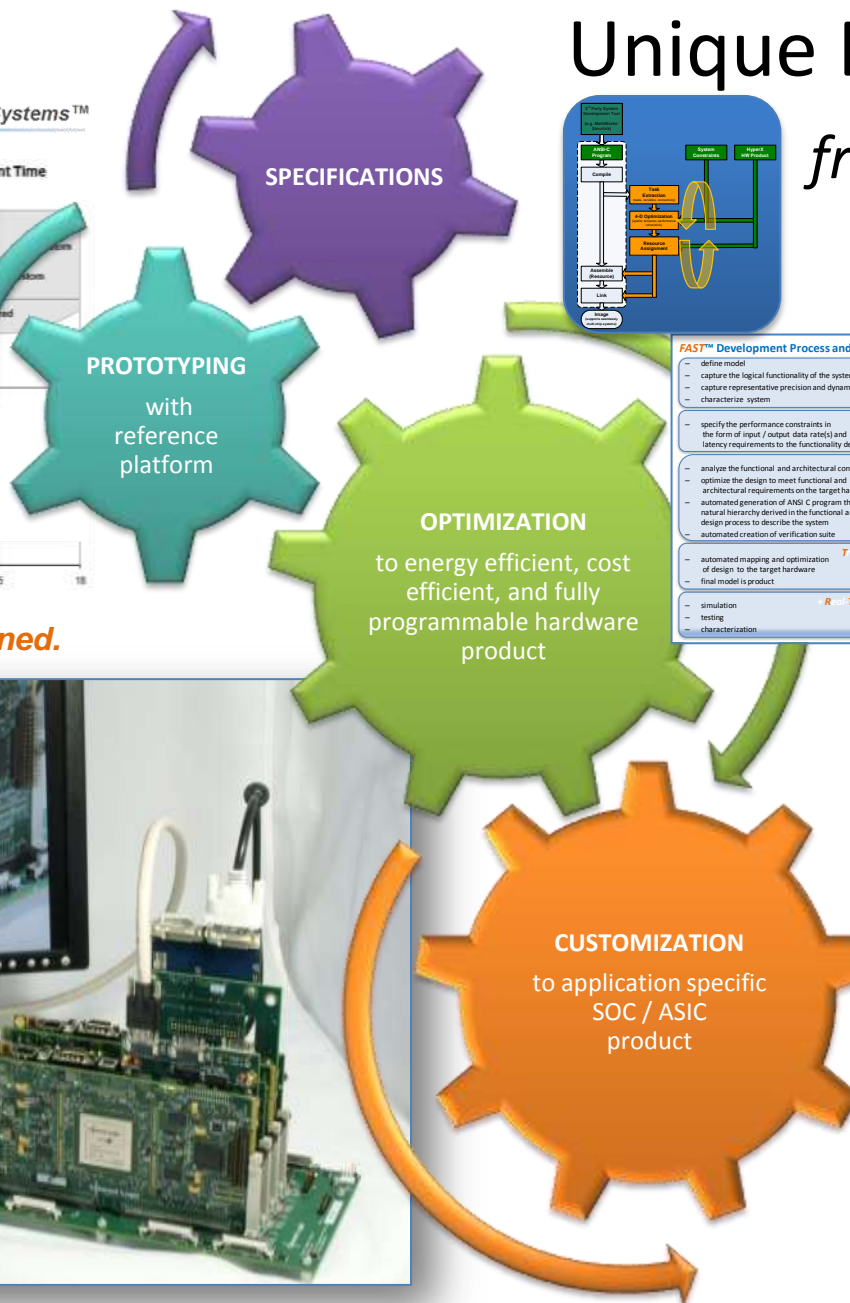- ❑ *Remote Sensor Platform*
- ❑ *Cryptography*

SPAWAR

CERDEC

Unique Design Flow

from Prototyping

to Product

Coherent Logix™
Enabling Low Power Software Defined Systems™

Mathematical OPs / Second / Watt versus Development Time
(all data memory movement encompassed in an OP)

Low Power Processing, Redefined.

SPECIFICATIONS

PROTOTYPING
with reference platform

OPTIMIZATION
to energy efficient, cost efficient, and fully programmable hardware product

CUSTOMIZATION
to application specific SOC / ASIC product

FAST™ Development Process and RTA™

- define model
- capture the logical functionality of the system
- capture representative precision and dynamic range
- characterize system

Functional Analysis

- specify the performance constraints in the form of input / output data rate(s) and latency requirements to the functionality defined

Architecture Constraints

- analyze the functional and architectural constraints
- optimize the design to meet functional and architectural requirements on the target hardware.
- automated generation of ANSI C program that represents natural hierarchy derived in the functional and system design process to describe the system
- automated creation of verification suite

System Design

- automated mapping and optimization of design to the target hardware
- final model is product

Transformation to Hardware

- simulation
- testing
- characterization

Real-Time Analysis

Prepare design
Task Extraction
Optimization
Resource Assignment

Design Selector

Tool Flow Steps

Tool Flow Cockpit & Process Feedback Window

System Performance View
Task Breakdown
Critical Path Analysis
Latency, Power, and Resource Trade-offs

System Communication View
Task Activity on Hardware
Data Routing

System Energy View
Resource Power
Power Optimization

System Centric View
Common Debugger
Cycle Accurate Simulator
Source Code, Variables
Breakpoint
Low level optimization

Coherent Logix™ HyperX™
hx3100™
1ERB37A0500C10
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Why we are interested in SHO?

- We are interested in supporting the hardware and software development infrastructure to support the experimentation and prototyping of 3D display systems with an eye towards providing production 3D display programmable processors.

- Questions?

- Contact Information:

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